REMARKS

Claims 1-30 were previously pending in this application. By this amendment, Applicant is canceling claim 15 without prejudice or disclaimer. Claims 1, 2, 8, 9, 16-21, 22, 27 and 28 have been amended. No new claims have been added. As a result claims 1-14 and 16-30 are pending for examination with claims 1, 8, 16, 22, 27 and 28 being independent claims. No new matter has been added.

Claims Objected To

The Examiner objected to claims 17-21 as depending from claim 15 and claiming a method even though claim 15 claimed digital signal processor. Claims 17-21 have been amended accordingly.

Rejections Under 35 U.S.C. §102

The Examiner rejected claims 1-30 under 35 U.S.C. §102(b) as being anticipated by Lomp (U.S. 5,799,010). Applicant respectfully disagrees and traverses as follows.

Each of the claims is directed to a method or apparatus for processing values in a digital signal processor. The Examiner rejected each claim based on Lomp, which discloses a code division multiple access (CDMA) communication system. In response to this rejection Applicant has amended the claims to more particularly point out the invention. In particular, certain claims were amended to clarify that the specified operations are executed in response to <u>a</u> <u>single instruction</u> in a digital signal processor.

As an example, claim 1 (emphasis added) reads:

1.   A method for processing a signal value in a digital signal processor, the method comprising:

in response to **a single instruction** that specifies at least a signal value and a despreading code decoding the signal value by:

performing a multiplication of bits of the signal value by bits of the despreading code,

performing an addition summing the results of the multiplication, and

storing the results of the addition.

Nowhere does Lomp disclose a single instruction specifying a value and a despreading code, where, in response to that single instruction, the signal is decoded as required by claim 1.

Lomp is directed to the architecture of a CDMA system and does not discuss processor level architecture. The present invention as defined by the claims is directed to operating a digital signal processor with a single instruction directed to multiplying signals by codes. Lomp does not contain any teaching regarding the instruction level operation of a digital signal processor and certainly does not teach or suggest the architecture necessary to operate on a signal and a code using only a single instruction. Lomp in Fig. 17 appears to disclose a hardware modem.

The present invention teaches and claims performing the code and signal operation in response to a single instruction. The use of a single instruction is not taught, disclosed or suggested by Lomp.

Furthermore, the additional independent claims require the operation in question to be performed in a single instruction.

Claim 8 requires that "in response to a single instruction that specifies at least a signal value and a set of codes" that the signal values be multiplied to the codes and the results summed to produce a data set. Lomp does not teach or suggest performing this operation in response to a single instruction.

Claim 16 is directed to a digital signal processor comprising a particular structure capable of decoding a data signal in the operation of a single instruction in a manner similar to claim 1. As discussed above, Lomp does not teach or suggest performing these operations in response to a single instruction.

Claims 22, 27, and 28 also claim methods for operating on a data signal value with a code value and performing a complex operation in response to a single instruction. Performing the method in response to a single instruction is not taught by Lomp.

As each of the independent claims, and therefore the dependent claims as well, require specified operations to be performed in response to a single instruction, the claims are therefore patentable over Lomp.

Accordingly, withdrawal of the rejection is respectfully requested.

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CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
Rifaat, et al., Applicants

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